CLAIMS

1. A method of encapsulating a semiconductor chip assembly having a top layer with an array of exposed terminals thereon, the terminals being electrically connected to the chip, said method comprising the steps of:

placing an encapsulant barrier adjacent the semiconductor chip assembly, said encapsulant barrier at least partially defining an encapsulation area;

providing a protective barrier for protecting the terminals on the top layer from an encapsulation material; and

introducing an encapsulation material into at least a portion of the encapsulation area so that the encapsulation material flows to fill the encapsulation area and then cures to a substantially solid condition, the protective barrier preventing the encapsulation material from contacting the terminals on the top layer.

2. The method in Claim 1, wherein said encapsulation material is a curable material which is in liquid form when introduced into said encapsulation area.

3. The method in Claim 2, further comprising the step of curing said curable material after said curable material has been introduced into said encapsulation area.

4. The method in Claim 3, wherein the curing step includes heating said curable material.

5. The method in Claim 3, wherein the hardening step includes mixing a plurality of mutually reactive materials to form said curable material during or before said curable material is introduced into said encapsulation area, whereby said curable material is at least partially cured by reaction of said mutually reactive materials.

6. The method in Claim 3, wherein said curable material is a curable elastomer.

7. The method in Claim 1, wherein said introducing step includes step of introducing a preform into said encapsulation area.

8. The method in Claim 7, wherein said introducing step includes heating said preform so that it liquefies and said encapsulation material flows substantially throughout the encapsulation area.

9. The method in Claim 1, wherein said placing step includes placing said encapsulant barrier a spaced distance from the periphery of said semiconductor chip.

10. The method in Claim 1, wherein said encapsulant barrier in said placing step is at least a portion of a mold, and further comprising the step of removing the mold after the encapsulation material is at least partially cured.

11. The method in Claim 1, wherein said encapsulant barrier in said placing step is at least a portion of a can which forms part of a package for the chip assembly, said can being secured to said chip subassembly.

12. The method in Claim 11, wherein said can includes a bottom in contact with the semiconductor chip and a wall extending upwardly from said bottom about the periphery of said semiconductor chip.

13. The method in Claim 12, wherein said can is made from aluminum or an aluminum alloy.

14. The method in Claim 12, further comprising the step of positioning said semiconductor chip assembly within said can via positioning means in said can.

15. The method in Claim 14, wherein said step of positioning includes centering said semiconductor chip assembly via said positioning means.

16. The method in Claim 1, wherein said encapsulant barrier in said placing step is at least a

portion of a ring which forms part of a package for the chip, said ring having a wall extending upwardly alongside said semiconductor chip assembly.

17. The method in Claim 1, wherein the introducing step is done before the placing step and includes associating a preform of an encapsulation material with the protecting barrier.

18. The method in Claim 17, wherein the providing step is done before the placing step.

19. The method in Claim 18, wherein said encapsulant barrier is a ring.

20. The method in Claim 1, wherein said top layer includes a top surface on which the array of terminals is disposed, and said barrier includes a dam extending upwardly from said top surface.

21. The method in Claim 20, wherein said providing step includes attaching said dam to said top surface.

22. The method in Claim 1, wherein said top layer includes a top surface on which the array of terminals are disposed, said protective barrier includes a sheetlike mask, and said providing step includes attaching said mask to said top surface of said top layer and to said encapsulant barrier such that said mask extends over said encapsulation area.

23. The method as claimed in Claim 22, wherein said encapsulant barrier includes a top edge substantially encircling said subassembly and said mask extends from said top surface of said top layer to said top edge of said encapsulant barrier.

24. The method in Claim 22, wherein said ~~substantially planar~~ sheetlike mask includes at least one opening in which the array of terminals are exposed.

25. The method in Claim 22, wherein said ~~substantially planar~~ sheetlike mask includes an array of terminal openings corresponding to said array of terminals on said top layer, and wherein said providing step includes aligning said array of terminal openings with said array

of terminals prior to attaching said mask to said top surface so that said terminals are exposed above said mask.

26. The method in Claim 25, wherein each of said array of terminal holes is sized such that said terminals fit closely in said terminal holes.

27. The method in Claim 26, wherein said ~~solder~~ mask is a dielectric.

28. The method in Claim 27, wherein said ~~solder~~ mask is an epoxy acrylic.

29. The method in Claim 22, wherein the providing step includes vacuum lamination of said ~~solder~~ mask to said top surface of said top layer and said encapsulant barrier.

30. The method in Claim 29, wherein said ~~solder~~ mask includes a fill hole communicating with said encapsulation area, and wherein said introducing step includes introduction of said encapsulant material via said ~~fill~~ hole.

31. The method in Claim 30, wherein said ~~solder~~ mask includes a vent hole communicating with said encapsulation area so that air does not become trapped in said encapsulation area during said introducing step.

32. The method in Claim 22, wherein said encapsulant barrier includes a fill hole, and said introducing step includes introduction of said encapsulation material via said fill hole.

33. The method in Claim 1, wherein said top layer is a spaced distance above said semiconductor chip, and further comprising the step of supporting said top layer above said semiconductor at least during said providing step.

34. The method in Claim 33, wherein said step of supporting said top layer includes providing a compliant layer between said top layer and said chip.

35. The method in Claim 1, wherein said protective barrier is a cap which engages by said top layer and covers said terminals.

36. The method in Claim 35, wherein said cap is metal.

37. The method in Claim 35, wherein said cap is plastic.

38. The method in Claim 35, wherein said cap is flexible and is forced against said top layer to prevent encapsulation material from contacting said terminals.

39. The method in Claim 1, wherein said encapsulant barrier is a ring having a top side, and further comprising the step of supporting said semiconductor chip assembly on a support surface and spacing said ring from said support surface such that the top side of said ring is at approximately the same height as the top surface of said top layer.

40. The method in Claim 39, wherein said spacing step includes the positioning of a spacer on said support surface adjacent said semiconductor chip assembly.

41. A method of encapsulating a semiconductor chip assembly having a top layer with an array of exposed terminals electrically connected to the chip, said method comprising the steps of:

placing an encapsulant barrier adjacent the semiconductor chip assembly, said encapsulant barrier at least partially defining an encapsulation area;

disposing a preform made of an encapsulation material in said encapsulation area, said preform normally being in a substantially solid state and being meltable to a temporary liquid state, said preform being of a predetermined volume which is equal to or less than the volume of said encapsulation area; and

liquifying said preform so that said encapsulation material flows substantially throughout said encapsulation area, but does not flow out of said

encapsulation area, at least in the area of the exposed terminals.

42. The method in Claim 41, wherein said encapsulation material is curable, and further comprising the step of hardening said encapsulation material after said encapsulation material has flowed substantially throughout said encapsulation area.

43. The method in Claim 42, wherein the liquifying step includes heating said preform, and said hardening step includes cooling said encapsulation material or allowing said encapsulation material to cool to the ambient temperature.

44. The method in Claim 41, wherein said preform is an extruded or injection molded bead of said encapsulation material.

45. The method in Claim 41, wherein said placing step includes placing said encapsulation barrier a space distance from the periphery of said semiconductor chip.

46. The method in Claim 41, wherein said encapsulation barrier is at least a portion of a can which forms part of a package for the chip.

47. The method in Claim 41, wherein said encapsulation barrier is at least a portion of a ring which forms part of a package for the chip.

48. A method of packaging a semiconductor chip assembly having a top layer, the top layer and semiconductor chip being spaced from one another by a gap, and the top layer having an array of exposed terminals electrically connected to the chip by leads, said method comprising the steps of:

placing an encapsulation barrier adjacent the semiconductor chip assembly, said encapsulation barrier at least partially defining an encapsulation area;

introducing an encapsulation material into at least a portion of said gap, such that said

encapsulation material is disposed between said top layer and said semiconductor chip; and

introducing an encapsulation material into at least a portion of the encapsulation area.

49. The method in Claim 48, wherein the encapsulation material in the introducing steps are the same encapsulation material.

50. The method in Claim 48, further comprising the step of providing a protective barrier for protecting the terminals on the top layer from an encapsulation material.

51. The method in Claim 50, further comprising the step of supporting said top layer above said semiconductor chip prior to providing said protective barrier.

52. The method in Claim 51, wherein the supporting step includes disposing support posts between said top layer and said semiconductor chip assembly.